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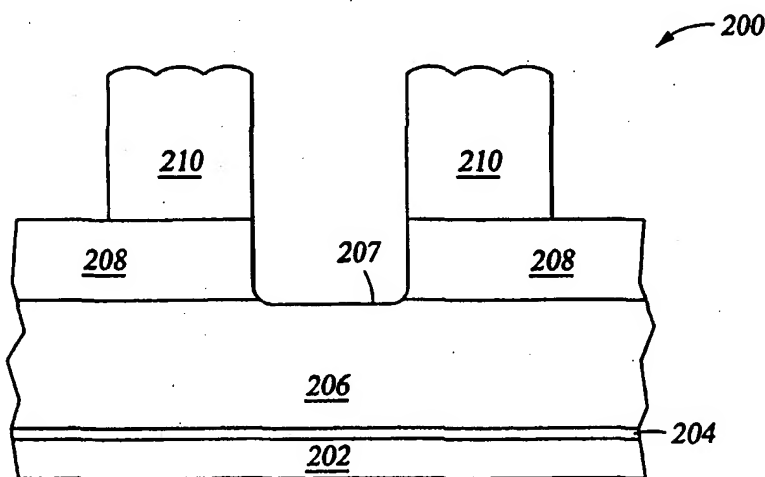
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(54) Title: METHOD OF ETCHING ORGANIC ANTIREFLECTION COATING (ARC) LAYERS



(57) Abstract: A two-step method of etching an organic coating layer, in particular, an organic antireflection coating (ARC) layer, is disclosed. During the main etch step, the organic coating layer, is etched using a plasma generated from a first source gas which includes a fluorocarbon and a non-carbon-containing, halogen-comprising gas. Etching is performed using a first substrate bias power. During the overetch step, residual organic coating material remaining after the main etch step is removed by exposing the substrate to a plasma generated from a second source gas which includes a chlorine-containing gas and an oxygen-containing gas, and

which does not include a polymer-forming gas. The overetch step is performed using a second substrate bias power which is less than the first substrate bias power. The first source gas and first substrate bias power provide a higher etch rate in dense feature areas than in isolated feature areas during the main etch step, whereas the second source gas and second substrate bias power provide a higher etch rate in isolated feature areas than in dense feature areas during the overetch step, resulting in an overall balancing effect.

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1 [0001] **METHOD OF ETCHING ORGANIC ANTIREFLECTION**
2 **COATING (ARC) LAYERS**

3 [0002] **BACKGROUND OF THE INVENTION**

4 [0003] 1. Field of the Invention

5 [0004] The present invention pertains to a method of etching organic antireflection
6 coatings (ARCs), and in particular, bottom antireflection coatings (BARCs). Organic
7 antireflection coatings, as indicated by their name, include carbon and hydrogen-containing
8 materials, and are typically polymeric in nature. The antireflection coatings are part of an
9 etch stack which is used to produce semiconductor devices, and they are pattern etched to
10 submicron dimensions. The present method permits control over shifts in the critical
11 dimension of the etched feature size, while providing uniform etching of ARCs across the
12 entire surface of a semiconductor substrate, despite variation in spacing between features
13 across the substrate surface.

14 [0005] 2. Brief Description of the Background Art

15 [0006] In the field of semiconductor device fabrication, it is well recognized that as
16 device feature sizes decrease to about 0.18 μm and smaller, mask patterning via photoresist
17 materials requires the use of deep ultra violet wavelength (DUV) imaging radiation.
18 Antireflective coatings are used in combination with DUV photoresists, among other
19 photoresists, to reduce standing waves and back-scattered light, so that the dimensions of
20 the patterning in the photoresist can be better controlled.

21 [0007] Generally, the photoresist is applied over a stack of other layers which are
22 patterned as a part of the semiconductor device fabrication process. Some of the layers in
23 the stack are consumed during the process of patterning underlying layers which become
24 part of the functioning device. An ARC layer may be present at a number of different
25 locations within a stack of layers, depending on the application. When the ARC layer is

1 applied over the top of a layer stack, it is referred to as a top antireflective coating (TAR).
2 When the ARC layer lies beneath the photoresist layer, it is commonly referred to as a
3 bottom antireflective coating (BARC). TAR coatings are frequently removed during the
4 photoresist patterning (developing) process, while BARC layers most often require a dry
5 etching removal step.

6 [0008] Processes for the dry etching of organic ARCs usually are accomplished in a
7 plasma etch system. ARC etching plasma source gases vary considerably in composition.
8 Some examples of plasma source gas combinations include $\text{CHF}_3/\text{CF}_4/\text{Ar-O}_2$; $\text{CF}_4/\text{He-O}_2$;
9 O_2/N_2 ; HBr/O_2 ; and $\text{HBr}/\text{CO}_2/\text{O}_2\text{-Ar}$.

10 [0009] In one process for etching organic antireflective coatings overlying a silicon-
11 containing substrate, the substrate is placed into a process chamber and treated with a
12 plasma. The plasma is generated from a process gas comprising oxygen and a compound
13 selected from a group of compounds consisting of hydrogen and bromine-containing
14 compounds, hydrogen and iodine-containing compounds, and mixtures thereof. Processing
15 variables are adjusted to provide anisotropic etching of the organic antireflective coating.

16 [0010] In another etching process, an anti-reflection coating overlying a semiconductor
17 substrate is etched by employing a plasma formed from a mixture of oxygen, nitrogen, and
18 at least one inert gas. In an alternative method, the antireflective coating layer may be
19 etched by employing a nitrogen plasma, which includes an inert gas, without any oxygen in
20 the plasma, although the etch rate is said to be reduced.

21 [0011] Another method for plasma etching a BARC layer overlying a semiconductor
22 substrate utilizes etch chemistry provided by a plasma processing gas which includes
23 hydrogen bromide (HBr), CO_2 , and O_2 , with argon or another inert gas.

24 [0012] More information regarding the kinds of processes described above may be found
25 in European Patent Publication No. EP 0820093, of Zhao et al., published January 21, 1998;
26 U.S. Patent No. 5,910,453, to Gupta et al., issued June 8, 1999; and European Patent

1 Application No. EP 0859400, of Yang et al., published August 19, 1998.

2 [0013] Uniformity of etching across a wafer has long been a concern, and, in general, the
3 references pertaining to etching of organic antireflective coating layers place great emphasis
4 on maintenance of the critical dimension of the feature being etched, such as a line width,
5 contact pad dimension, gate size, and so on. Emphasis is also placed on the selectivity of
6 the etch process, where the etch rate of an ARC layer is compared with the etch rate of an
7 adjacent layer of material, such as a silicon-containing layer underlying the ARC layer, for
8 example.

9 [0014] A very important variable, which has become more important with decreasing
10 critical dimension size of etched features, is the etched feature critical dimension uniformity
11 control across a substrate, such as a semiconductor wafer. For example, when the pattern
12 being etched into an ARC layer is a series of lines and spaces, and the spacing between the
13 lines is different at different positions on the substrate surface, the etch rate of the ARC may
14 vary at different positions on the substrate surface. This may affect the depth of etch and
15 may affect the profile of the feature being etched. It also affects the critical dimension
16 uniformity across the substrate. The phenomenon of a change in overall etch performance
17 across a substrate surface as a function of the spacing between etched features is sometimes
18 referred to as a "microloading" effect. Differences in etch rate and/or etched feature profile
19 occur in part because the availability of etchant species at a given position on the substrate
20 surface varies, and the amount of etch byproduct which is produced varies as well. One of
21 the reasons that the availability of etchant species and byproduct residue varies across a
22 wafer surface is that the input and distribution of processing gases and the removal of
23 processing gases and etch byproducts from the processing chamber is frequently not
24 uniform. Another reason is that there is different spacing between pattern features at
25 different locations (positions) on the substrate surface. Etch byproducts tend to be generated
26 by two different mechanisms: 1) the use of etchant gas compositions which contain

1 significant amounts of passivating gases (e.g., N₂, or polymer-generating gases, such as
2 carbon-containing gases), and/or 2) back-sputtering of etched material onto feature sidewalls
3 during etching. Etchant gas-generated passivation layers (1) tend to build up on feature
4 sidewalls relatively evenly over the substrate surface. Back-sputtered passivation layers (2)
5 tend to deposit more on isolated feature areas of the substrate, where there is more back-
6 sputtering because the amount of material being etched tends to be greater than in dense
7 feature areas of the substrate.

8 [0015] Commonly owned, copending U.S. Application Serial No. 09/611,085, of Shen
9 et al., discloses a process for plasma etching of ARC layers which is said to provide critical
10 dimension uniformity across a substrate surface. The ARC etching process utilizes CF₄,
11 HBr, and O₂ chemistry. However, while this process provides excellent critical dimension
12 uniformity across a substrate surface during etching of 1500 Å thick BARC layers, critical
13 dimension uniformity is not as good when the process is used to etch thicker (e.g., 2000 Å)
14 BARC layers. This is believed to be due to the longer etch time needed to etch a thicker
15 BARC layer. Therefore, it would be desirable to provide a process for etching a BARC
16 layer that would provide excellent critical dimension uniformity across a substrate surface,
17 when etching thicker (> 1500 Å thickness) BARC layers.

18 [0016] SUMMARY OF THE INVENTION

19 [0017] The present invention includes a method of etching organic coating layers, and
20 in particular, antireflective coating layers. The method provides improved critical dimension
21 uniformity of the etched feature across the substrate surface, while providing selectivity
22 favoring etching of the antireflective coating layer relative to an underlying silicon-
23 containing layer. The present method has been shown to provide excellent critical
24 dimension uniformity during etching of thicker (> 1500 Å) organic coating layers.

1 [0018] We have discovered a method for etching an organic coating layer which provides
2 unexpected control over the etched feature critical dimension, as well as the critical
3 dimension uniformity across a substrate surface (CD shift range), despite a difference in the
4 spacing between etched features over the substrate surface.

5 [0019] A two-step method is used to etch an organic coating layer. The first step of the
6 method is a main etch step, during which essentially the entire thickness of the organic
7 coating layer is etched to endpoint. The main etch utilizes a plasma generated from a first
8 source gas comprising a fluorocarbon gas and a non-carbon-containing, halogen-comprising
9 gas.

10 [0020] The second step of the method is an overetch step, during which residual coating
11 layer material remaining on feature surfaces following the main etch step is removed. The
12 overetch step utilizes a plasma generated from a second source gas comprising a chlorine-
13 comprising gas, an oxygen-comprising gas, and an inert gas (*i.e.*, a noble gas). This
14 chemistry provides excellent ($> 20 : 1$) selectivity for etching the organic coating layer
15 relative to an underlying silicon-containing layer. Power applied to bias the substrate during
16 the overetch step is less than the power applied to bias the substrate in the main etch step.

17 [0021] With reference to a pattern of lines and spaces (by way of example and not
18 limitation), the etch chemistry and process conditions used in the main etch step produces
19 a smaller etched line width in dense areas (where features are spaced closer together) than
20 the etched line width in isolated areas (where features are spaced further apart). Typically,
21 the etched line width in both the dense areas and the isolated areas is smaller than the line
22 width of the photoresist used to pattern the organic coating layer (such as an ARC). This
23 reduction in line width from the target line width is referred to as a "negative CD shift" or
24 a "CD loss". Thus, the negative CD shift is greater in the dense areas than in the isolated
25 areas during the main etch. The negative CD shift across the substrate is referred to as the
26 "CD shift range".

1 [0022] As discussed above, the total amount of material being etched in isolated areas
2 is greater than in dense areas; therefore, more polymeric material redeposits and builds up
3 on isolated feature sidewalls during etching. This polymeric material build-up forms
4 passivation layers which inhibit sidewall etching and slow the etch rate of isolated features.
5 Further, the chemistry used in the main etch step includes CF_4 , which forms polymers which
6 contribute to the build-up of passivation layers on isolated feature sidewalls during etching.

7 [0023] The etch chemistry and process conditions used in the overetch step produce a
8 negative CD shift in the isolated areas which is greater than the negative CD shift in the
9 dense areas. This is the opposite of the effect observed during the main etch step. Because
10 most of the organic coating layer material has already been etched in the main etch step,
11 build-up of passivation layers in isolated areas due to polymer deposition is no longer as
12 much of a factor in the overetch step as it was during the main etch step. Further, the etch
13 chemistry used in the overetch step does not include a polymer-producing (passivating)
14 plasma source gas.

15 [0024] Another important processing variable is the substrate bias power used in the
16 main etch step compared with the overetch step. The power applied to the substrate is lower
17 in the overetch step than in the main etch step. As a result, there is less driving force to
18 direct etchant species toward the substrate surface during the overetch step, which tends to
19 slow the etch rate. This effect is more pronounced in dense feature areas than in isolated
20 areas, because the narrower spacing between features in dense areas (higher aspect ratio)
21 tends to protect exposed etched sidewall features from impacting reactive species.
22 Therefore, the combination of etch chemistry and application of less substrate bias in the
23 overetch step produces more rapid etching in isolated feature areas than in dense areas
24 during the overetch step. Thus, there is a balancing effect when the main etch step is
25 combined with the overetch step. This balancing effect reduces the CD shift range.

1 [0025] In summary, the present invention utilizes multiple etching steps which
2 compensate for each other and take advantage of different mechanisms to achieve uniformity
3 of etching across a substrate surface. Accordingly, disclosed herein is a method of etching
4 an organic coating layer on a semiconductor substrate which utilizes a combination of the
5 etch chemistries and substrate bias powers used in the main etch and overetch steps to
6 balance etching in dense and isolated areas of a semiconductor substrate.

7 [0026] **BRIEF DESCRIPTION OF THE DRAWINGS**

8 [0027] Figure 1A shows a schematic of a preferred embodiment plasma processing
9 apparatus of the kind which can be used to carry out the etching processes described herein.

10 [0028] Figure 1B shows a schematic of a substrate surface, indicating the bottom, left,
11 center, right, and top locations of a substrate relative to the schematic of the processing
12 apparatus shown in Figure 1A.

13 [0029] Figure 2A shows an etch stack 200 which represents a starting structure of the
14 kind upon which the method of the present invention is performed. The etch stack 200
15 includes, from top to bottom, a patterned layer 210 of photoresist, an organic antireflection
16 coating (ARC) layer 208, a polysilicon layer 206, and a silicon oxide gate dielectric layer
17 204, all deposited on a silicon substrate 202. The relative thicknesses of the film stack
18 layers are not shown to scale.

19 [0030] Figure 2B shows the etch stack 200 after performance of the main etch step
20 according to the method of the invention. The entire thickness of the ARC layer 208 has
21 been etched to endpoint using a first plasma source gas, and an upper surface 207 of
22 polysilicon layer 206 has been exposed. Residual ARC material overlies the polysilicon

1 layer surface 207 on certain areas of the substrate surface.

2 [0031] Figure 2C shows the etch stack 200 after performance of the overetch step
3 according to the method of the invention. Residual ARC material has been removed from
4 the polysilicon layer surface 207, without any significant etching of the polysilicon layer.

5 [0032] Figure 3 shows a graph 300 of the shift 302 in critical dimension of the etched
6 feature (*i.e.*, the difference between the line width of the etched ARC and the line width in
7 the photoresist used to pattern the ARC) as a function of the spacing 304 between etched
8 features, at various locations on a substrate surface, when a plasma source gas of CF_4 , HBr ,
9 and O_2 was used to etch the organic ARC layer.

10 [0033] Figure 4 shows a graph 400 of the shift 402 in critical dimension of the etched
11 feature (as measured in dense and isolated areas of the substrate) as a function of the
12 thickness 404 of the BARC layer, when a plasma source gas of CF_4 , HBr , and O_2 was used
13 to etch the organic ARC layer.

14 [0034] Figure 5 shows a graph 500 of the shift 502 in critical dimension of the etched
15 feature as a function of the spacing 504 between etched features, at various locations on a
16 substrate surface, when a plasma source gas of CF_4 , Cl_2 , and N_2 was used to etch the organic
17 ARC layer.

18 [0035] Figure 6 shows a graph 600 of the shift 602 in critical dimension of the etched
19 feature as a function of the spacing 604 between etched features, at various locations on a
20 substrate surface, when a plasma source gas of Cl_2 , O_2 , and Ar was used to etch the organic
21 ARC layer.

1 [0036] Figure 7 shows a graph 700 of the shift 702 in critical dimension of the etched
2 feature as a function of the spacing 704 between etched features, at various locations on a
3 substrate surface, when a main etch chemistry of CF_4 and Cl_2 , and an overetch chemistry of
4 Cl_2 , O_2 , and Ar, were used to etch the organic ARC layer.

5 [0037] Figure 8 is a schematic of an Applied Materials' MXP+ polysilicon etch chamber,
6 which is an alternative example of an apparatus of the kind which can be used to carry out
7 the etching processes described herein.

8 [0038] **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

9 [0039] The present disclosure provides a two-step method of etching an organic coating
10 layer, such as an organic antireflection coating (ARC) layer. The method provides excellent
11 critical dimension (CD) uniformity across a substrate surface, despite a variation in spacing
12 between features across the substrate surface.

13 [0040] The first step of the method is a main etch step, during which essentially the entire
14 thickness of the organic coating layer is etched to endpoint. The main etch utilizes a plasma
15 generated from a first source gas comprising a fluorocarbon gas and a non-carbon-
16 containing, halogen-comprising gas. The fluorocarbon gas is typically CF_4 , but may
17 alternatively be, for example, CHF_3 , CH_2F_2 , C_2F_6 , C_4F_8 , or a combination thereof. The non-
18 carbon-containing, halogen-comprising gas is typically Cl_2 , but may alternatively be, for
19 example, HBr, HCl, or any combination of Cl_2 , HBr, and/or HCl.

20 [0041] A first source gas comprising CF_4 and Cl_2 works particularly well. Typically, the
21 volumetric ratio of CF_4 : Cl_2 in the first source gas ranges from about 1 : 1 to about 6 : 1,
22 preferably, from about 2 : 1 to about 5 : 1. If needed, a minor amount of a passivating gas,
23 such as N_2 or HBr, may be included in the CF_4/Cl_2 source gas combination.

1 [0042] In an alternative, less preferred embodiment of the invention, a first source gas
2 comprising CF_4 , HBr , and O_2 may be used to perform the main etch step. This particular
3 combination of main etch plasma source gases produces an increase in the negative CD shift
4 in comparison with the CF_4/Cl_2 source gas combination.

5 [0043] A substrate bias power within the range of about 30 W to about 90 W is typically
6 used during the main etch step.

7 [0044] The etch chemistry and process conditions used during the main etch step provide
8 a higher etch rate in dense feature areas than in isolated feature areas of a semiconductor
9 substrate.

10 [0045] The second step of the method is an overetch step, during which residual coating
11 layer material remaining on feature surfaces following the main etch step is removed.

12 [0046] The overetch step utilizes a plasma generated from a second source gas
13 comprising a chlorine-comprising gas, an oxygen-comprising gas, and an inert gas (*i.e.*, a
14 noble gas). The chlorine-comprising gas is typically Cl_2 . The chlorine-comprising gas is
15 typically Cl_2 , but may alternatively be, for example, HCl . The oxygen-comprising gas is
16 typically O_2 , which may be provided as He/O_2 (where O_2 is about 30 volume % of the He/O_2
17 mixture). The inert gas is typically argon, but may alternatively be a different noble gas, for
18 example, helium, neon, xenon, krypton, or the inert gas may be a combination of noble
19 gases. Typically, the volumetric ratio of $\text{Cl}_2 : \text{O}_2$ in the second source gas ranges from about
20 2 : 3 to about 3 : 1, preferably, from about 1 : 1 to about 3 : 1. In addition, the argon in the
21 second source gas typically ranges from about 20 volume % to about 80 volume %, preferably,
22 from about 30 volume % to about 50 volume %.

23 [0047] The substrate bias power used in the overetch step is lower than that used in the
24 main etch step. An overetch substrate bias power that is less than 80%, and preferably less
25 than 70%, of the substrate bias power used in the main etch step works particularly well.

1 [0048] An organic antireflection coating (ARC) layer is frequently part of a
2 semiconductor structure, where the ARC layer overlies a layer of a silicon-containing
3 material, such as polysilicon, which further overlies a gate dielectric layer. In order to avoid
4 significant overetching of the ARC layer and pitting of the underlying polysilicon layer, the
5 second source gas preferably provides a selectivity of at least 10 : 1 for etching the organic
6 coating layer relative to polysilicon. (The term "selectivity" is typically used to refer to a
7 ratio of etch rates of two materials.) It is important to avoid pitting of the polysilicon layer,
8 because this pitting will transfer directly to the underlying (thin) dielectric layer during
9 subsequent polysilicon layer etching and may cause a punch-through of the thin dielectric
10 layer.

11 [0049] The chemistry and process conditions used in the main etch step produce a greater
12 negative CD shift in dense feature areas than in isolated feature areas. The overetch
13 chemistry and process conditions produce a greater negative CD shift in isolated feature
14 areas than in dense feature areas, on the substrate. The main etch and the overetch thus
15 counteract each other, resulting in a reduced CD shift range across the substrate surface and
16 providing improved critical dimension uniformity across the substrate surface.

17 [0050] As a preface to the detailed description, it should be noted that, as used in this
18 specification and the appended claims, the singular forms "a", "an", and "the" include plural
19 referents, unless the context clearly dictates otherwise.

20 [0051] I. AN APPARATUS FOR PRACTICING THE INVENTION

21 [0052] The embodiment example etch processes described herein were carried out in a
22 Centura® Integrated Processing System available from Applied Materials, Inc., of Santa
23 Clara, California. The system is shown and described in United States Patent No. 5,583,737
24 to Collins et al., the disclosure of which is hereby incorporated by reference. Although the
25 etch process chamber used to process the substrates described in the Examples presented

1 herein is shown in schematic in Figure 1, any of the etch processors available in the industry
2 should be able to take advantage of the etch chemistry described herein, with some
3 adjustment to other process parameters.

4 [0053] The equipment shown in schematic in Figure 1 includes a Decoupled Plasma
5 Source (DPS) of the kind described by Yan Ye et al. at the Proceedings of the Eleventh
6 International Symposium of Plasma Processing, May 7, 1996 and as published in the
7 Electrochemical Society Proceedings, Volume 96-12, pp. 222 - 233 (1996). Figure 1 is a
8 schematic of an individual CENTURA® DPST™ polysilicon etch chamber 102 of the type
9 used in the Applied Materials' CENTURA® polysilicon etch system. The CENTURA®
10 DPST™ polysilicon etch chamber 100 is configured to be mounted on a standard
11 CENTURA® etch mainframe.

12 [0054] The CENTURA® DPST™ polysilicon etch chamber 100 consists of an upper
13 chamber 104 having a ceramic dome 106, and a lower chamber 108. The lower chamber 108
14 includes a monopolar electrostatic chuck (ESC) cathode 110. Gas is introduced into the
15 chamber via gas injection nozzles 114 for uniform gas distribution. Chamber pressure is
16 controlled by a closed-loop pressure control system (not shown) with a throttle valve 118.
17 During processing, a substrate 120 is introduced into the lower chamber 108 through inlet
18 122. The substrate 120 is held in place by means of a static charge generated on the surface
19 of electrostatic chuck (ESC) cathode 110 by applying a DC voltage to a conductive layer
20 located under a dielectric film on the chuck surface. The cathode 110 and substrate 120 are
21 then raised by means of a wafer lift 124 and a seal is created against the upper chamber 104
22 in position for processing. Etch gases are introduced into the upper chamber 104 via the
23 ceramic gas injection nozzles 114. The polysilicon etch chamber 100 uses an inductively
24 coupled plasma source power 126 and matching network 128 operating at 12.56 MHZ which
25 is connected to inductive coil 134 for generating and sustaining a high density plasma. The
26 wafer is biased with an RF source 130 and matching network 132 operating at 13.56 MHZ.

1 Power to the plasma source 126 and substrate biasing means 130 are controlled by separate
2 controllers (not shown).

3 [0055] The temperature on the surface of the etch chamber walls is controlled using
4 liquid-containing conduits (not shown) which are located in the walls of the etch chamber
5 100. The temperature of the semiconductor substrate is controlled by stabilizing the
6 temperature of the electrostatic chuck cathode 110 upon which the substrate 120 rests. The
7 helium gas is used to facilitate heat transfer between the substrate and the pedestal. During
8 the etch process, the substrate 120 surface is gradually heated by the plasma to a steady state
9 temperature which is approximately 10 to 40°C higher than the substrate support platen
10 temperature, depending on the process conditions. It is estimated that the substrate surface
11 temperature was typically around 40°C to 85°C during most of our experiments. The surface
12 of the etching chamber 100 walls was maintained at about 65°C using the cooling conduits
13 previously described. The ceramic dome 106 was maintained at a temperature of about
14 80°C.

15 [0056] When the end point of an etch is signaled by the etch reaching an interface with
16 a different material, an endpoint subsystem (not shown) senses the end of the etch process
17 by monitoring changes in the light emitted by the plasma in the etch chamber 100. Data is
18 then displayed on a PC monitor. The operator sets an algorithm which controls the endpoint
19 system.

20 [0057] Figure 1B shows a schematic of a substrate 120 surface 140, including the bottom
21 142, left 144, center 146, right 148, and top 150 surface locations on substrate 120 (a silicon
22 wafer in this case), relative to a notch 152 located at the bottom 142 of the substrate 120.
23 These surface locations are shown, relative to the schematic of the processing apparatus 100
24 shown in Figure 1B, where arrow 154 indicates the direction toward vacuum throttle valve
25 118, arrow 156 indicates the direction toward inlet 122, and substrate 120 is shown resting
26 on upper surface 158 of electrostatic chuck 110.

[0058] Alternatively, the method of the invention may be performed in an etch processing apparatus wherein power to a plasma generation source and power to a substrate biasing means are controlled by a single power control, such as the Applied Materials' MXP or MXP+ polysilicon etch chamber. Figure 8 is a schematic of an Applied Materials' MXP+ polysilicon etch chamber 800, which is a parallel plate plasma etch chamber of the kind which is well-known in the art. The MXP+ polysilicon etch chamber offers advantages over other similar etch chambers in that it includes a simplified, two-dimensional gas distribution plate 802, which allows for more uniform gas distribution throughout the chamber. Another modification is a removable aluminum chamber liner 804, which can be easily removed and replaced during each wet cleaning procedure, allowing for a more rapid cleaning cycle. Yet another modification is an improved focus ring 806, which moves together with (rather than independently from) the cathode 808, resulting in reduced particle generation due to fewer moving parts within the apparatus. The high temperature cathode 808 has independent temperature control (not shown), which functions in response to a temperature reading from pedestal temperature probe 812, which permits operation at a temperature in excess of the process chamber temperature. The substrate to be processed (not shown) rests on an electrostatic chuck pedestal 810, which is joined to cathode 808.

[0059] II. THE METHOD OF THE INVENTION FOR ETCHING ORGANIC ANTIREFLECTION COATING (ARC) LAYERS

[0060] Prior to performing the method of the invention, one must first provide a starting etch stack. A typical etch stack is described below.

[0061] Figure 2A shows an etch stack 200 which represents a starting structure of the kind upon which the method of the present invention is performed. The pattern is one of lines and spaces, and Figure 2A illustrates a cross-sectional schematic of these lines and spaces.

[0062] Etch stack 200 includes the following layers, from top to bottom: a patterned layer 210 of photoresist; an organic antireflection coating (ARC) layer 208; a silicon-containing

1 layer 206; and a gate dielectric layer 204, all deposited on a substrate 202.

2 [0063] The thickness and patterning method for the photoresist layer 210 will depend on
3 the particular photoresist material used and the pattern to be imaged in the photoresist.
4 Photoresist layer 210 may be any suitable photoresist material known in the art. Typically,
5 the photoresist is an organic, carbon-containing material. Frequently, a deep ultra-violet
6 (DUV) photoresist is used to transfer a pattern to a substrate. A typical film thickness for
7 such a DUV photoresist ranges from about 4000 Å to about 6000 Å. In the starting etch stack
8 etched in the Examples below, the photoresist 210 was a DUV photoresist having a thickness
9 of about 6000 Å. DUV photoresists are available from either JSR® or SHIPLEY®, INC., for
10 example, and not by way of limitation.

11 [0064] An ARC layer is frequently required when a DUV photoresist is used, to reduce
12 standing waves and back-scattered light in general during the photoresist imaging process.
13 Organic ARCs are preferred in some instances because they are more compatible with
14 photoresists. The organic ARC layer 208 may be formed from any of the organic ARC
15 materials known in the art, using conventional methods known in the art, such as a spin-on
16 technique. The organic ARC layer 208 typically has a thickness within the range of about
17 300 Å to about 3000 Å. In the starting etch stack etched in the Examples below, the organic
18 ARC layer 208 had a thickness of about 2000 Å.

19 [0065] The silicon-containing layer 206 is typically polysilicon or amorphous silicon. If
20 desired (such as to provide a low resistance gate structure), the silicon-containing layer 206
21 may be doped. The silicon-containing layer 206 is typically formed to have a thickness
22 within the range of about 1500 Å to about 3000 Å. In the starting etch stack etched in the
23 Examples below, the silicon-containing layer 206 was polysilicon, which was deposited
24 using a chemical vapor deposition (CVD) technique known in the art. Polysilicon layer 206
25 had a thickness of about 2000 Å.

1 [0066] Underlying polysilicon layer 206 is a thin gate dielectric layer 204, which is
2 typically an inorganic oxide, such as silicon oxide, silicon oxynitride, or tantalum pentoxide,
3 for example. Alternatively, the gate dielectric layer may be an organic dielectric, such as a
4 Poly(arylene)ether, a Poly(arylene)ether oxazole, Parylene-N, a Polyimide,
5 Polynaphthalene-N, a Polyphenyl-Quinoxaline, a Polybenzoxazole, Polyindane,
6 Polynorborene, Polyphenyleneoxide, or an α C, for example.

7 [0067] A silicon oxide gate dielectric layer 204 is typically formed to have a thickness
8 within the range of about 15 Å to about 100 Å. Other materials having different electrical
9 properties may be applied at a different thickness. For example, in the starting etch stack
10 etched in the Examples below, the gate dielectric layer 204 was silicon oxide, which had a
11 thickness of about 60 Å. When tantalum pentoxide is used, the thickness of the gate
12 dielectric layer may be lower than when silicon oxide is used. Such gate dielectric layers are
13 typically formed or deposited using conventional methods known in the art, such as thermal
14 oxidation or plasma-enhanced chemical vapor deposition (PECVD).

15 [0068] The substrate 202 is typically silicon, but may alternatively be glass or silicon-on-
16 insulator (SOI), for example. When the substrate is silicon, the silicon-containing layer 206
17 may be either polysilicon or amorphous silicon. However, when a glass substrate is used,
18 the silicon-containing layer 206 must be amorphous silicon, because, in order to form
19 polysilicon, an underlying silicon substrate is needed as a seed layer. Amorphous silicon can
20 be deposited using conventional physical vapor deposition (PVD) or chemical vapor
21 deposition (CVD) techniques.

22 [0069] According to one method of the invention, a main etch step is performed to etch
23 through essentially the entire thickness of organic ARC layer 208, exposing an upper surface
24 207 of polysilicon layer 206, as illustrated in Figure 2B. The main etch step preferably
25 utilizes a plasma generated from a source gas comprising CF_4 and Cl_2 . If needed, a minor
26 amount of a passivating gas such as N_2 may be included in the first plasma source gas.

1 [0070] In an alternative, less preferred embodiment of the invention, a first source gas
2 comprising CF_4 , HBr , and O_2 can be used to perform the main etch step. Compatible process
3 conditions for use with this chemistry are described in detail in commonly owned, copending
4 U.S. Application Serial No. 09/611,085, of Shen et al., which is hereby incorporated by
5 reference in its entirety.

6 [0071] The endpoint of the main etch step is detected using a an optical emission
7 spectroscopy (OES) endpoint detection system, at a wavelength of 4390 Å.

8 [0072] Referring to Figure 2C, an overetch step is then performed to remove residual
9 ARC material which remains on polysilicon layer surface 207 at the completion of the main
10 etch step. The plasma source gas used in the overetch step preferably provides a selectivity
11 of at least 10 : 1 for etching the organic ARC layer 208 relative to polysilicon layer 206, in
12 order to avoid significant overetching with the potential of pitting the surface of the
13 polysilicon layer 206. If the surface 207 of polysilicon layer 206 is pitted, this pitting may
14 transfer to the underlying gate dielectric layer 204. We have found that a plasma generated
15 from a chlorine-comprising gas, an oxygen-comprising gas, and an inert gas (*i.e.*, a noble gas)
16 provides a selectivity of at least 20 : 1 for etching an organic ARC material relative to
17 polysilicon.

18 [0073] Typical process condition ranges for the main etch and overetch steps are provided
19 in Table One, below.

[0074] Table One. Typical Process Conditions for Organic ARC Layer
Main Etch and Overetch

Process Condition	Main Etch	Overetch
Total Gas Flow (sccm)	100 - 200	50 - 200
CF ₄ (sccm)	50 - 150	--
Cl ₂ (sccm)	10 - 100	10 - 100
N ₂ (sccm)	0 - 50	--
O ₂ (sccm)	--	10 - 50
Argon (sccm)	--	20 - 100
Plasma Source Power (W)	200 - 600	200 - 600
Substrate Bias Power (W)	30 - 90*	20 - 60*
Process Chamber Pressure (mTorr)	3 - 10	3 - 10
Substrate Temp. (°C)	30 - 65	30 - 65
Etch Time (sec)	30 - 120	5 - 40
Plasma Density (e ⁻ /cm ³)	≥ 1 x 10 ¹¹	≥ 1 x 10 ¹¹

* Where the substrate biasing power applied in the overetch step is lower than the substrate biasing power applied in the main etch step.

[0075] III. EXAMPLES

[0076] The experiments described in the Examples below were performed using the etch stack 200 shown in Figure 2A, as follows (layers listed from top to bottom): a 6000 Å DUV photoresist layer 210 (previously patterned); a 2000 Å organic ARC layer 208; a 200 Å polysilicon layer 206; and a 60 Å silicon oxide gate dielectric layer 204, all deposited on a silicon substrate 202. The etch stack was prepared using conventional techniques known in the art, as described above.

[0077] COMPARATIVE EXAMPLE ONE:

[0078] The ARC layer 208 was etched using a plasma source gas of CF₄, HBr, and O₂. Process conditions, such as gas flow rates and bias power, were varied between experiments. The plasma source gas used during Run #3 also included N₂; the plasma source gas used during Run #4 included argon (rather than nitrogen).

[0079] Table Two provides experimental process conditions and critical dimension data generated during etching of the ARC layer.

[0080] Table Two. BARC Etching Using CF₄, HBr, and O₂

Run #	1	2	3	4	5	6
CF ₄ (sccm)	60	60	60	30	60	80
HBr (sccm)	20	20	20	10	20	20
O ₂ (sccm)	40	40	40	20	20	40
N ₂ (sccm)	--	--	30	--	--	--
Ar (sccm)	--	--	--	60	--	--
Source Power (W)	300	300	300	300	300	300
Bias Power (W)	90	75	90	90	90	90
Chamber Pressure (mTorr)	4	4	4	4	4	4
Endpoint* (sec)	38.0	43.1	42.8	45.6	47.2	41.6
Overetch (sec)	7.6	8.6	8.5	9.1	9.4	8.3
Average CD Shift (nm)	-44.4	-51.9	-45.6	-37.8	-22.5	-39.9
CD Shift Range (nm)	14.8	13.3	13.6	15.8	20.8	14

* Endpoint determined by optical emission spectroscopy (OES).

1 [0081] Referring to Table Two, above, the term "CD shift" refers to the difference
2 between the line width of the etched ARC and the line width in the photoresist used to pattern
3 the ARC. Thus, a positive CD shift indicates that the etched CD is larger than the pattern CD
4 prior to etch. A negative CD shift (also referred to as "CD loss") indicates that the etched CD
5 is smaller than the pattern CD prior to etch. "Average CD shift" refers to an average of CD
6 shift measurements taken at various locations (e.g., top, center, bottom) on the substrate and
7 for various feature spacings (dense vs. isolated).

8 [0082] "CD shift range" refers to the difference between the highest measured CD shift
9 and the lowest measured CD shift, and is an indication of CD uniformity across the substrate
10 surface. Variations in CD shift (indicated by the CD shift range) may be attributable to either
11 geographic considerations (i.e., the location on the substrate surface) or demographic
12 considerations (i.e., the spacing between the lines being etched). While it is highly desired
13 to have a minimal CD shift, it is critical that the CD shift be consistent between different
14 substrate locations and different feature spacings. If the CD shift (i.e., the difference between
15 the line width of the etched ARC and the line width in the photoresist used to pattern the
16 ARC) is relatively high, but the variation in CD shift (CD shift range) is low, this means that
17 etching is occurring consistently across the substrate surface, and the etching process can be
18 adjusted to compensate for the CD shift. However, it is very difficult to compensate for a
19 high variation in CD shift, which signifies that the etching process is not consistent across
20 the substrate surface.

21 [0083] Figure 3 shows a graph 300 of the shift in critical dimension of the etched feature
22 as a function of the spacing between etched features, for Run # 1. The shift in critical
23 dimension (in μm) is shown on the axis labeled 302, for an etched line in a pattern of lines
24 and spaces. The shift in critical dimension is shown as a function of the spacing between the
25 lines (in μm), on the axis numbered 304. There are four plots on the graph: plot 306
26 represents a bottom location on a substrate, plot 308 represents a location on the left side of

1 the substrate, plot 310 represents a center location on the substrate, and plot 312 represents
2 a top location on the substrate, as illustrated with reference to Figure 1B.

3 [0084] Graph 300 makes it possible to look at the variation in critical dimension shift
4 which is attributable to the location on the substrate surface and the variation in critical
5 dimension shift which is attributable to differences in spacing between the lines being etched.
6 Referring to Figure 3, it is easy to see that the CD shift due to differences in spacing is much
7 greater than the CD shift due to location on the substrate surface. The highest CD shift
8 appears to be about $-0.050\ \mu\text{m}$, and the lowest CD shift appears to be about $-0.035\ \mu\text{m}$, for
9 a CD shift range of approximately $0.015\ \mu\text{m}$ (measured value: $14.8\ \text{nm}$). The average
10 critical dimension shift was $-44.4\ \text{nm}$. There is a trend toward greater CD loss in dense areas
11 (*i.e.*, areas having smaller space widths) of the substrate.

12 [0085] Due to the size reduction in semiconductor device structures, device fabricators
13 are looking for a critical dimension shift variation (CD shift range) across the substrate (CD
14 uniformity) of about $10\ \text{nm}$ ($0.01\ \mu\text{m}$) or less. An average CD shift of $30\ \text{nm}$ ($0.03\ \mu\text{m}$) or
15 less is also desired. As indicated in Table Two, none of the combinations of plasma source
16 gas composition and process conditions used during Runs # 1 - 6 provided both the desired
17 CD shift range and an acceptable average CD shift. In fact, there appeared to be a trade-off
18 between average CD shift and CD shift range. As the average CD shift decreased, the CD
19 uniformity across the substrate (as indicated by CD shift range) worsened (refer to Run # 5).
20 When the CD shift range was relatively low (indicating acceptable uniformity), the average
21 CD shift was unacceptably high (refer to Run # 2).

22 [0086] Figure 4 shows a graph 400 of the shift in critical dimension of the etched feature
23 as a function of the thickness of the BARC layer, for Run # 1. The shift in critical dimension
24 (in μm) is shown on the axis labeled 402, for an etched line in a pattern of lines and spaces.
25 The shift in critical dimension is shown as a function of the thickness of the BARC layer
26 (in \AA), on the axis numbered 404. There are two plots on the graph: plot 406 represents

1 isolated lines on the substrate, and plot 408 represents a dense array of lines. As shown in
2 Figure 4, CD shift was acceptable ($\leq 0.03 \mu\text{m}$) when thinner BARC layers were etched.
3 However, CD shift in both dense and isolated areas of the substrate increased as the thickness
4 of the BARC layer increased above 1500 \AA . This is believed to be due to the longer etch
5 time needed to etch through a thicker BARC layer. It should also be noted that there is an
6 increasing divergence between isolated 406 and dense 408 lines as the BARC layer thickness
7 increases, indicating a worsening CD shift range.

8 [0087] EXAMPLE TWO:

9 [0088] Upon reviewing the critical dimension data obtained for BARC etching using a
10 plasma source gas of CF_4 , HBr , and O_2 , we determined that a new BARC etch process that
11 would provide acceptable CD shift and CD uniformity during etching of thicker (*i.e.*, greater
12 than 1500 \AA) BARC layers was needed.

13 [0089] The ARC layer 208 of the etch stack shown in Figure 2A and described above was
14 etched using a plasma source gas of CF_4 , Cl_2 , and N_2 . Process conditions, such as plasma
15 source power and bias power, were varied between experiments. The plasma source gas used
16 during Run # 13 also included argon; the plasma source gas used during Run # 12 did not
17 include N_2 .

18 [0090] Table Three provides experimental process conditions and critical dimension data
19 generated during etching of the ARC layer.

[0091] Table Three. BARC Etching Using CF₄, Cl₂, and N₂

Run #	7	8	9	10	11	12	13	14
CF ₄ (sccm)	100	100	100	100	100	100	100	100
Cl ₂ (sccm)	20	20	20	20	20	20	20	20
N ₂ (sccm)	20	20	20	20	20	0	20	20
Ar (sccm)	--	--	--	--	--	--	10	--
Source Power (W)	315	315	500	315	250	315	315	315
Bias Power (W)	50	50	50	90	40	50	50	30
Chamber Pressure (mTorr)	4	4	4	4	4	4	4	4
Endpoint* (sec)	62	64.8	52	49.3	78.2	52	59	76.6
Overetch (sec)	18	12.9	11	9.8	15.6	20	8	15.3
Average CD Shift (nm)	-19.2	-16.2	-22.2	4.5	-16.4	-18.5	-21.8	-25.8
CD Shift Range (nm)	17.2	18	23.3	44.7	18.3	15.9	18.9	15.7

* Endpoint determined by optical emission spectroscopy (OES).

[0092] As indicated in Table Three, none of the combinations of plasma source gas composition and process conditions used during Runs # 7 - 14 provided both the desired CD shift range (≤ 10 nm) and an acceptable average CD shift (≤ 30 nm). As also observed in Runs # 1 - 6, there appeared to be a trade-off between average CD shift and CD shift range. As the average CD shift decreased, the CD uniformity (as indicated by CD shift range) worsened (refer to Run # 10). When the CD shift range was relatively low (indicating acceptable uniformity), the average CD shift was unacceptably high (refer to Run # 14).

[0093] Figure 5 shows a graph 500 of the shift in critical dimension of the etched feature as a function of the spacing between etched features, for Run # 14. The shift in critical dimension (in μm) is shown on the axis labeled 502, for an etched line in a pattern of lines and spaces. The shift in critical dimension is shown as a function of the spacing between the

lines (in μm), on the axis numbered 504. There are five plots on the graph: plot 506 represents a bottom location on a substrate, plot 508 represents a location on the left side of the substrate, plot 510 represents a center location on the substrate, plot 512 represents a location on the right side of the substrate, and plot 514 represents a top location on the substrate.

[0094] Again, the CD shift due to differences in spacing is much greater than the CD shift due to location on the substrate surface. The CD shift range was 15.7 nm, with an average CD shift of -25.8. Again, there was a trend toward greater CD loss in dense areas (*i.e.*, areas having smaller space widths between features) of the substrate.

[0095] EXAMPLE THREE:

[0096] We decided to investigate the use of a chlorine and oxygen-based plasma for etching organic BARC layers. The experiment summarized in Table Four, below, utilized a plasma source gas of Cl_2 , O_2 , and argon.

[0097] Table Four. BARC Etching Using Cl_2 , O_2 , and Argon

Run #	15
Cl_2 (sccm)	18
O_2 (sccm)	18
Ar (sccm)	20
Source Power (W)	210
Bias Power (W)	33
Chamber Pressure (mTorr)	3
Endpoint* (sec)	74.7
Overetch (sec)	15
Average CD Shift (nm)	-26.6
CD Shift Range (nm)	18.6

* Endpoint determined by optical emission spectroscopy (OES).

[0098] Figure 6 shows a graph 600 of the shift in critical dimension of the etched feature as a function of the spacing between etched features, for Run # 15. The shift in critical dimension (in μm) is shown on the axis labeled 602, for an etched line in a pattern of lines and spaces. The shift in critical dimension is shown as a function of the spacing between the lines (in μm), on the axis numbered 604. There are five plots on the graph: plot 606 represents a bottom location on a substrate, plot 608 represents a location on the left side of the substrate, plot 610 represents a center location on the substrate, plot 612 represents a location on the right side of the substrate, and plot 614 represents a top location on the substrate.

[0099] The CD shift range was 18.6 nm, with an average CD shift of 26.6. However, the use of the $\text{Cl}_2/\text{O}_2/\text{Ar}$ etch chemistry in Run # 15 resulted in a trend toward greater CD loss in isolated areas (*i.e.*, areas having larger space widths between features) of the substrate, which was the opposite of the trend toward greater CD loss in dense areas observed when either the $\text{CF}_4/\text{HBr}/\text{O}_2$ (Runs # 1 - 6) or $\text{CF}_4/\text{Cl}_2/\text{N}_2$ (Runs # 7 - 14) etch chemistries were used.

[0100] The $\text{Cl}_2/\text{O}_2/\text{Ar}$ etch chemistry provided excellent ($> 20 : 1$) selectivity for etching the BARC layer 208 relative to the underlying polysilicon layer 206.

[0101] EXAMPLE FOUR:

[0102] The next set of experiments involved using a first etch chemistry for the BARC main etch, followed by a second etch chemistry for the overetch step. The main BARC etch utilized a plasma source gas of CF_4 and Cl_2 , optionally in combination with N_2 (in Runs # 16 - 18). The overetch step utilized a plasma source gas of Cl_2 , O_2 , and argon. Process conditions, such as gas flow rates, plasma source power, and bias power, were varied between experiments.

[0103] Table Five provides experimental process conditions for both the main BARC etch and overetch steps, as well as critical dimension data generated during etching of the ARC layer.

[0104] Table Five. BARC Etching Using CF₄/Cl₂ Main Etch and Cl₂/O₂/Ar Overetch

Run #	16	17	18	19	20	21	22
Main Etch Chemistry (sccm)	100 CF ₄ 20 Cl ₂ 20 N ₂	100 CF ₄ 20 Cl ₂ 20 N ₂	100 CF ₄ 20 Cl ₂ 10 N ₂	100 CF ₄ 20 Cl ₂	100 CF ₄ 20 Cl ₂	100 CF ₄ 20 Cl ₂	100 CF ₄ 20 Cl ₂
Source Power (W)	315	315	315	315	315	315	315
Bias Power (W)	30	30	50	50	60	50	50
Chamber Pressure (mTorr)	4	4	4	4	4	4	4
Endpoint (sec)	77.7	74.6	56.8	50.8	47.6	51.8	50.8
Overetch Chemistry (sccm)	18 Cl ₂ 18 O ₂ 20 Ar	18 Cl ₂ 18 O ₂ 20 Ar	18 Cl ₂ 18 O ₂ 20 Ar	18 Cl ₂ 18 O ₂ 20 Ar	18 Cl ₂ 18 O ₂ 20 Ar	18 Cl ₂ 12 O ₂ 20 Ar	18 Cl ₂ 18 O ₂ 20 Ar
Source Power (W)	210	300	300	300	300	300	300
Bias Power (W)	33	30	30	30	30	30	30
Chamber Pressure (mTorr)	3	3	3	3	3	3	3
Endpoint (sec)	15	10	7	10	10	10	10
Average CD Shift (nm)	-34.0	-35.3	-22.8	-26.2	-24.3	-29.2	-28.2
CD Shift Range (nm)	13.8	13.1	14.7	8.5	11.9	11.2	9.5

[0105] As discussed above, the CF_4/Cl_2 etch chemistry shows a trend toward greater CD loss in dense areas, whereas the $\text{Cl}_2/\text{O}_2/\text{Ar}$ etch chemistry shows a trend toward greater CD loss in isolated areas of the substrate. As shown in Table Five, above, the microloading trends of the main etch and overetch chemistries appear to compensate for each other, resulting in improved CD uniformities across the substrate. Runs # 19 and 22 (which utilized the same plasma source gas composition and process conditions) provided average CD shifts of less than 30 nm and CD shift ranges of less than 10 nm.

[0106] Figure 7 shows the shift in critical dimension of the etched feature as a function of the spacing between etched features, for Run # 19. The shift in critical dimension (in μm) is shown on the axis labeled 702, for an etched line in a pattern of lines and spaces. The shift in critical dimension is shown as a function of the spacing between the lines (in μm), on the axis numbered 704. There are five plots on the graph: plot 706 represents a bottom location on a substrate, plot 708 represents a location on the left side of the substrate, plot 710 represents a center location on the substrate, plot 712 represents a location on the right side of the substrate, and plot 714 represents a top location on the substrate.

[0107] The improved CD uniformity obtained using the ARC etch method of the invention can be clearly seen in the graph 700 in Figure 7, when compared with the CD uniformity data shown in any of the preceding Figures 3, 4, 5, and 6.

[0108] The above described preferred embodiments are not intended to limit the scope of the present invention, as one skilled in the art can, in view of the present disclosure expand such embodiments to correspond with the subject matter of the invention claimed below.

CLAIMS

We claim:

1. A method of etching an organic coating layer, comprising the following steps:
 - a) a main etch step, wherein essentially the entire thickness of said organic coating layer is etched using a plasma generated from a first source gas comprising a fluorocarbon gas and a non-carbon-containing, halogen-comprising gas; and
 - b) an overetch step, wherein residual organic coating material remaining after said main etch step is removed by exposing said residual organic coating material to a plasma generated from a second source gas comprising a chlorine-comprising gas, an oxygen-comprising gas, and an inert gas.
2. The method of Claim 1, wherein said fluorocarbon gas is selected from the group consisting of CF_4 , CHF_3 , CH_2F_2 , C_2F_6 , C_4F_8 , and combinations thereof.
3. The method of Claim 2, wherein said fluorocarbon gas is CF_4 .
4. The method of Claim 1, wherein said non-carbon-containing, halogen-comprising gas is selected from the group consisting of Cl_2 , HBr , and HCl .
5. The method of Claim 4, wherein said non-carbon-containing, halogen-comprising gas is Cl_2 .

- 1 6. The method of Claim 3, wherein said first source gas comprises CF_4 and Cl_2 .
- 1 7. The method of Claim 6, wherein a volumetric ratio of CF_4 : Cl_2 in said first source
2 gas ranges from about 1 : 1 to about 6 : 1.
- 1 8. The method of Claim 6, wherein said first source gas further comprises a
2 passivating gas selected from the group consisting of N_2 and HBr .
- 1 9. The method of Claim 3, wherein said first source gas comprises CF_4 , HBr , and O_2 .
- 1 10. The method of Claim 1, wherein said chlorine-comprising gas is selected from the
2 group consisting of Cl_2 and HCl .
- 1 11. The method of Claim 10, wherein said chlorine-comprising gas is Cl_2 .
- 1 12. The method of Claim 1, wherein said oxygen-comprising gas is O_2 .
- 1 13. The method of Claim 1, wherein said inert gas is selected from the group consisting
2 of argon, helium, xenon, krypton, and combinations thereof.
- 1 14. The method of Claim 13, wherein said inert gas is argon.
- 1 15. The method of Claim 11, wherein said second source gas comprises Cl_2 , O_2 , and
2 argon.

16. The method of Claim 15, wherein a volumetric ratio of $\text{Cl}_2 : \text{O}_2$ in said second source gas ranges from about 2 : 3 to about 3 : 1.
17. The method of Claim 15, wherein argon comprises from about 20 volume % to about 80 volume % of said second source gas.
18. The method of Claim 17, wherein argon comprises from about 30 volume % to about 50 volume % of said second source gas.
19. The method of Claim 1, wherein said a substrate bias power used in said overetch step is less than a substrate bias power used in said main etch step.
20. The method of Claim 19, wherein said substrate bias power used in said overetch step is 80% or less of said substrate bias power used in said main etch step.
21. The method of Claim 1, wherein said organic coating layer is an antireflective coating (ARC) layer.
22. The method of Claim 21, wherein said second source gas provides a selectivity of at least 20 : 1 for etching said ARC layer relative to an underlying silicon-containing layer.
23. The method of Claim 22, wherein said underlying silicon-containing layer is polysilicon.
24. The method of Claim 1, wherein said organic coating layer has a thickness of at least 1500 Å.

25. A method of etching an organic coating layer on a semiconductor substrate, comprising the following steps:

a) a main etch step, wherein essentially the entire thickness of said organic coating layer is etched using a plasma generated from a first source gas, wherein etching is performed using a first substrate bias power, and wherein said main etch step provides a higher etch rate in dense feature areas of said substrate than in isolated feature areas of said substrate; and

b) an overetch step, wherein residual organic coating material remaining after said main etch step is removed by exposing said substrate to a plasma generated from a second source gas, wherein etching is performed using a second substrate bias power which is less than said first substrate bias power, and wherein said overetch step provides a higher etch rate in isolated feature areas of said substrate than in dense feature areas of said substrate.

26. The method of Claim 25, wherein said second substrate bias power is 80% or less of said first substrate bias power.

27. The method of Claim 26, wherein said second substrate bias power is 70% or less of said first substrate bias power.

28. The method of Claim 25, wherein said first source gas comprises a fluorocarbon gas and a non-carbon-containing, halogen-comprising gas.

29. The method of Claim 28, wherein said first source gas comprises CF_4 and Cl_2 .

30. The method of Claim 29, wherein said first source gas further comprises a passivating gas selected from the group consisting of N_2 and HBr.

31. The method of Claim 25, wherein said second source gas comprises a chlorine-comprising gas, an oxygen-comprising gas, and an inert gas.

32. The method of Claim 31, wherein said second source gas comprises Cl_2 , O_2 , and argon.

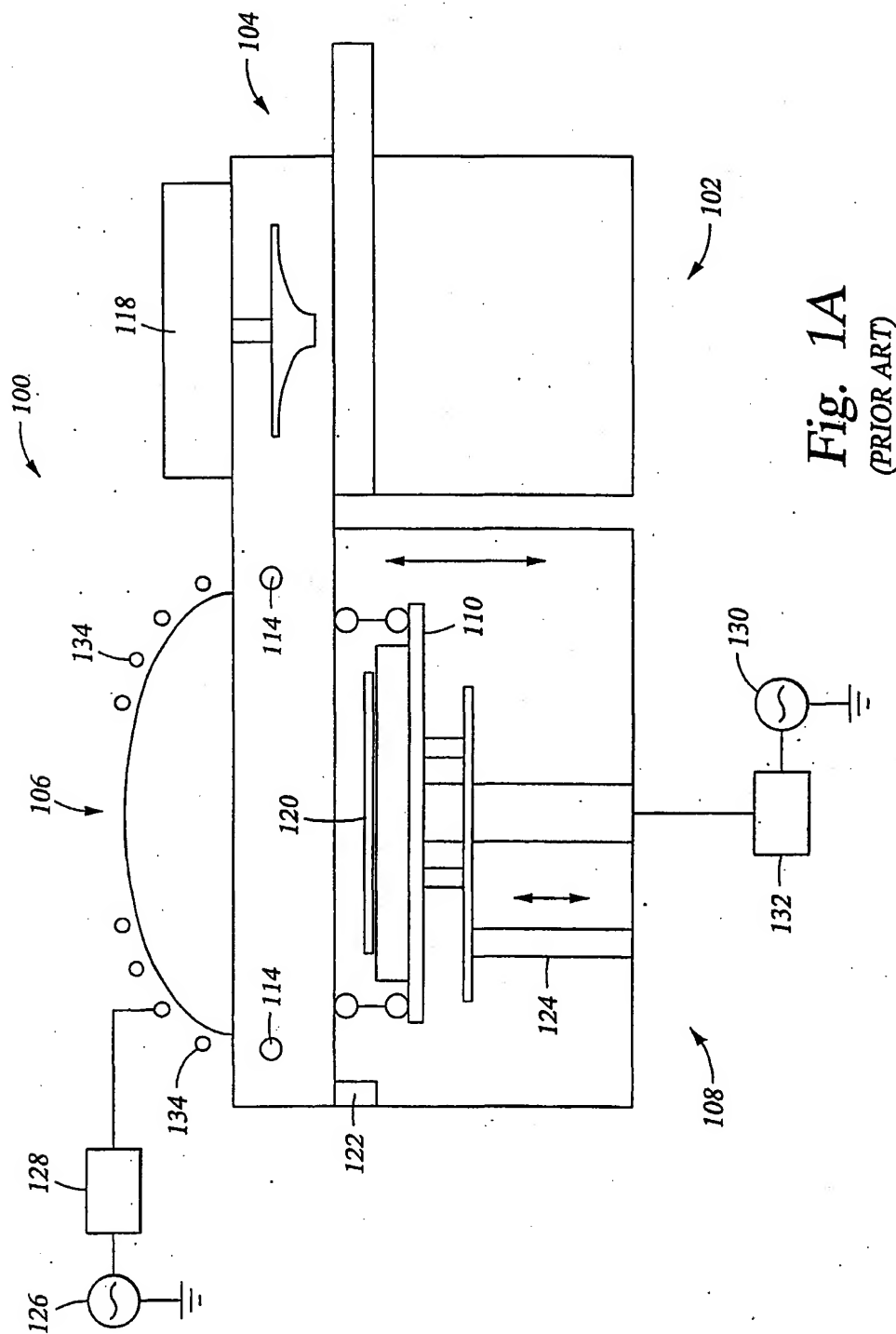
33. The method of Claim 25, wherein said organic coating layer is an antireflective coating (ARC) layer.

34. The method of Claim 33, wherein said second source gas provides a selectivity of at least 20 : 1 for etching said ARC layer relative to an underlying silicon-containing layer.

35. The method of Claim 34, wherein said underlying silicon-containing layer is polysilicon.

36. The method of Claim 35, wherein said organic coating layer has a thickness of at least 1500 Å.

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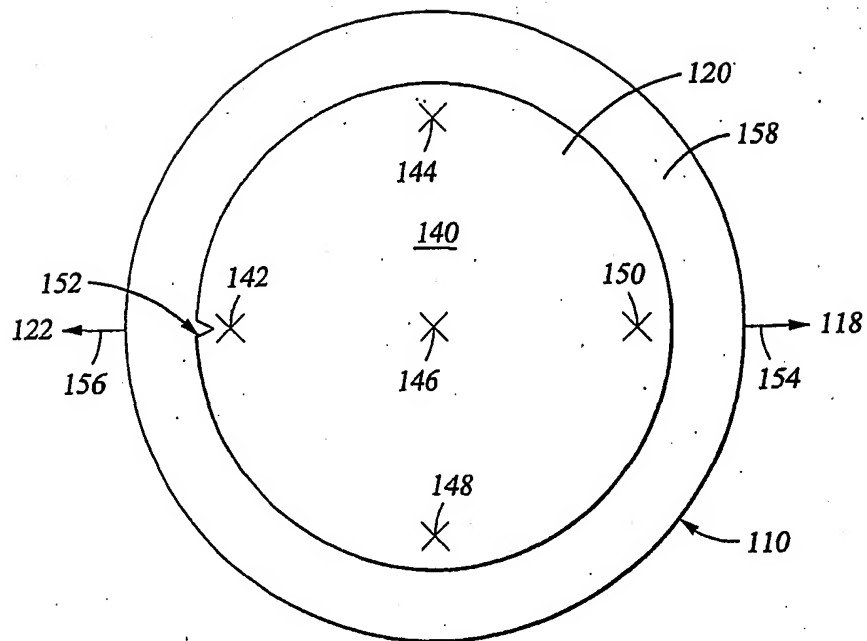


Fig. 1B

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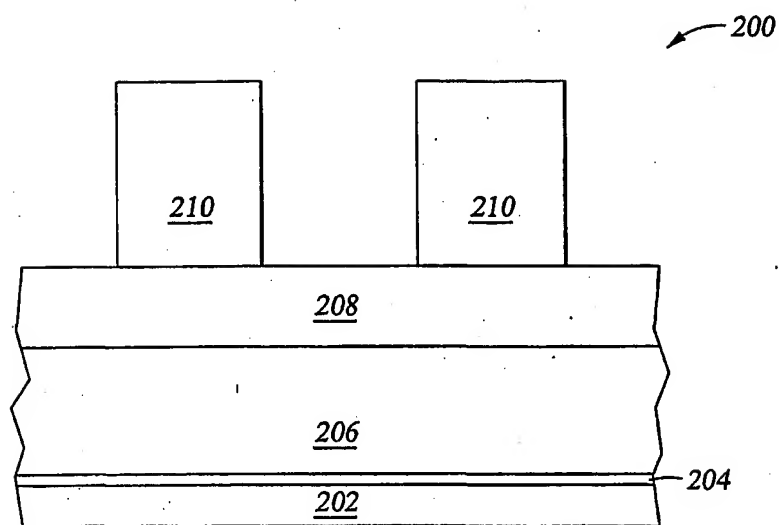


Fig. 2A

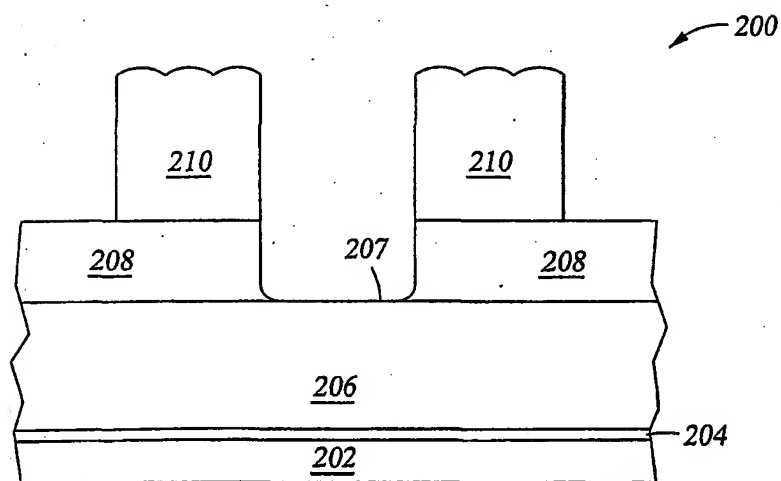


Fig. 2B

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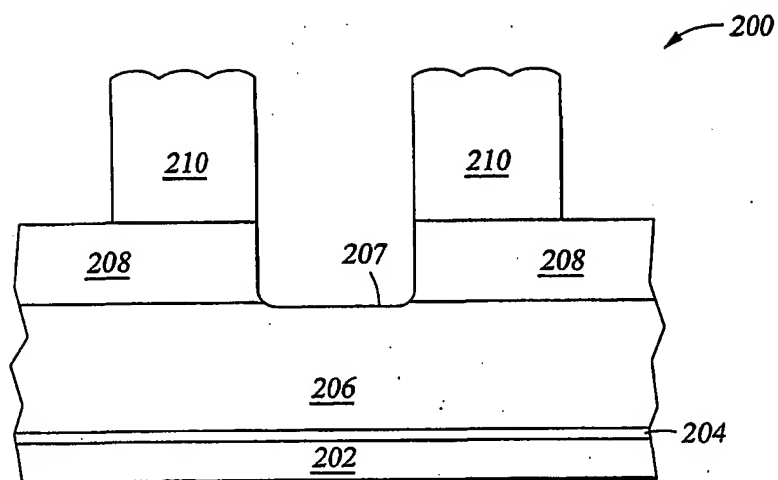


Fig. 2C

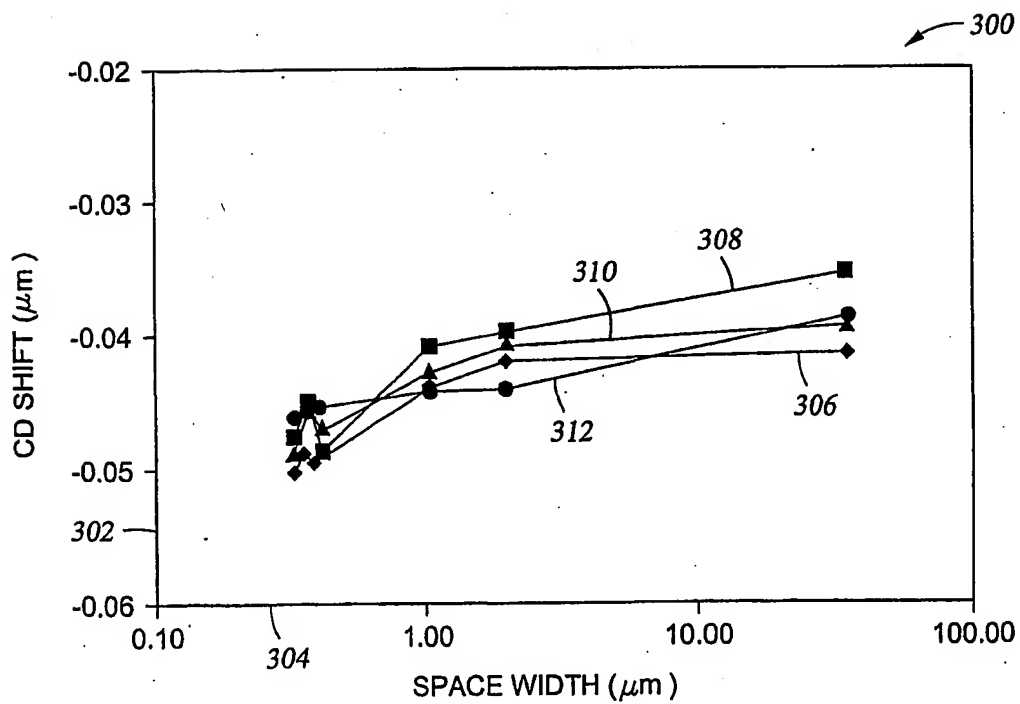
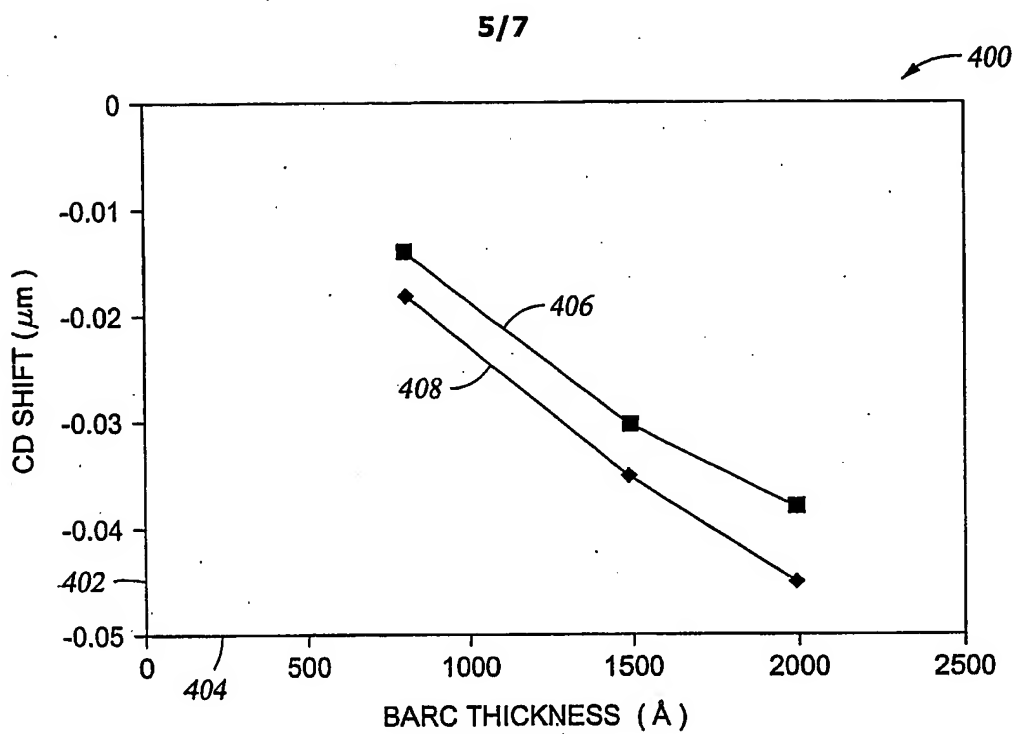
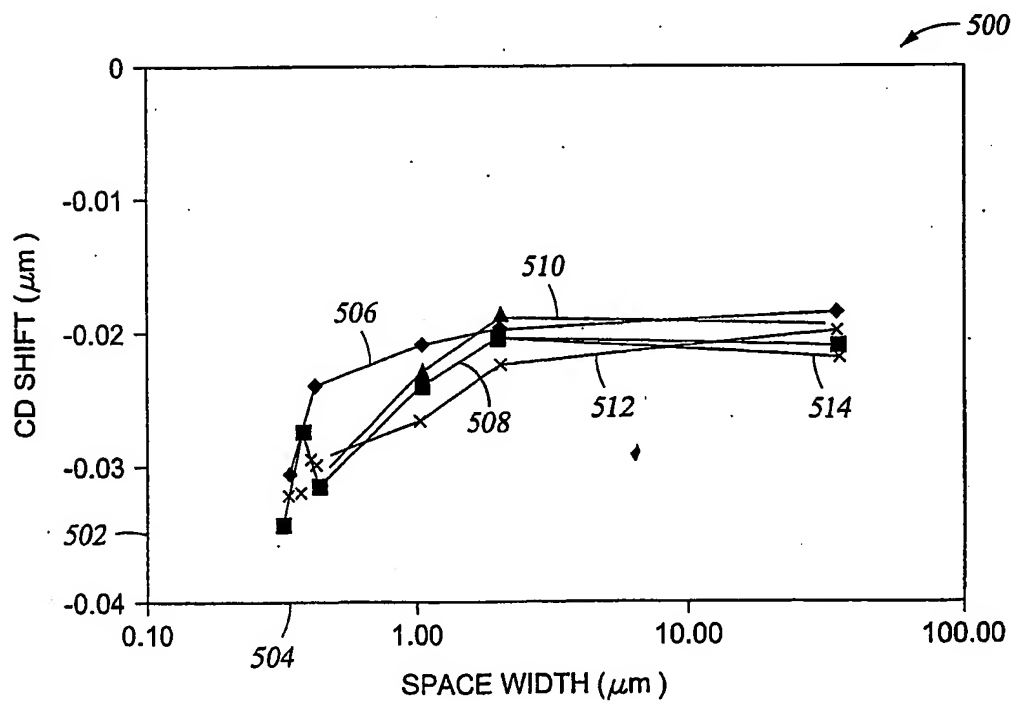
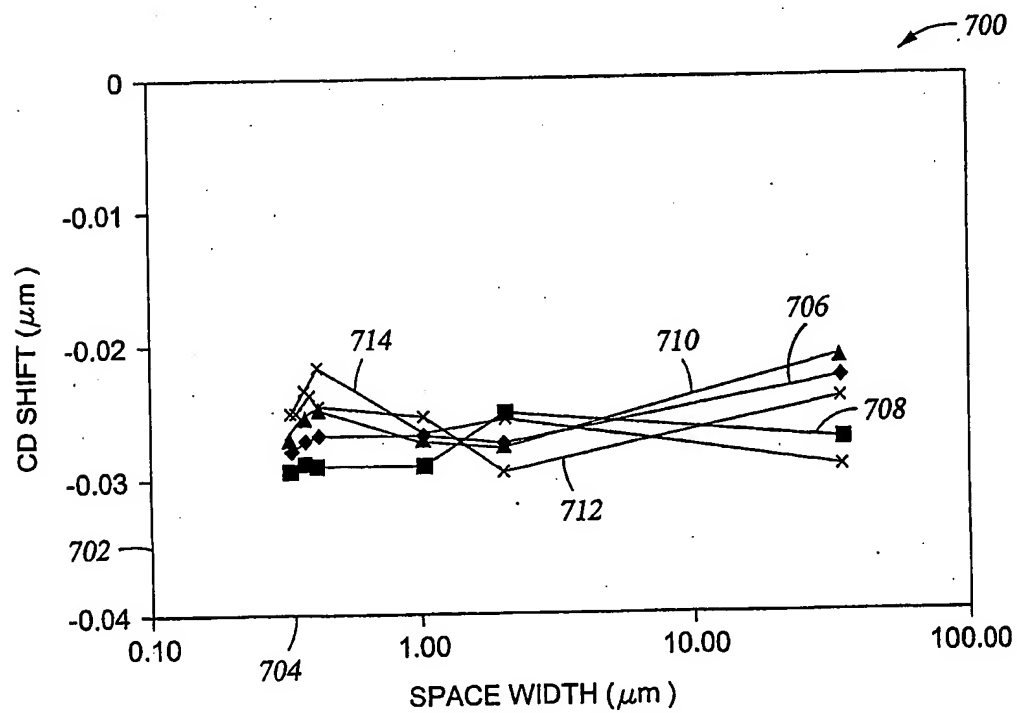
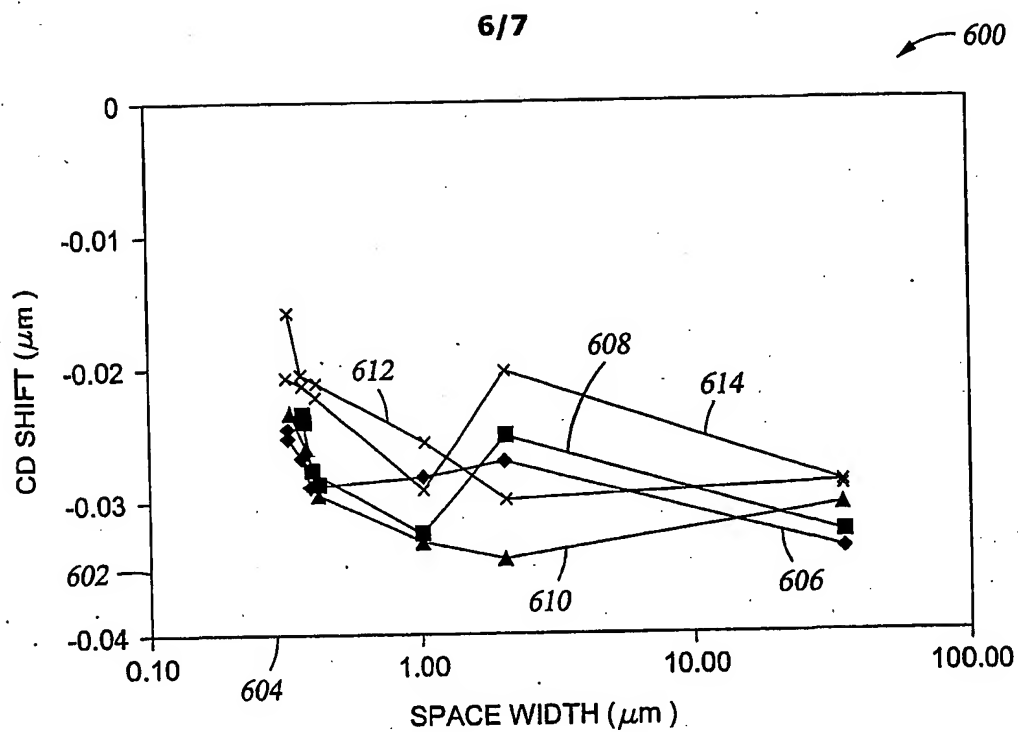


Fig. 3

*Fig. 4**Fig. 5*



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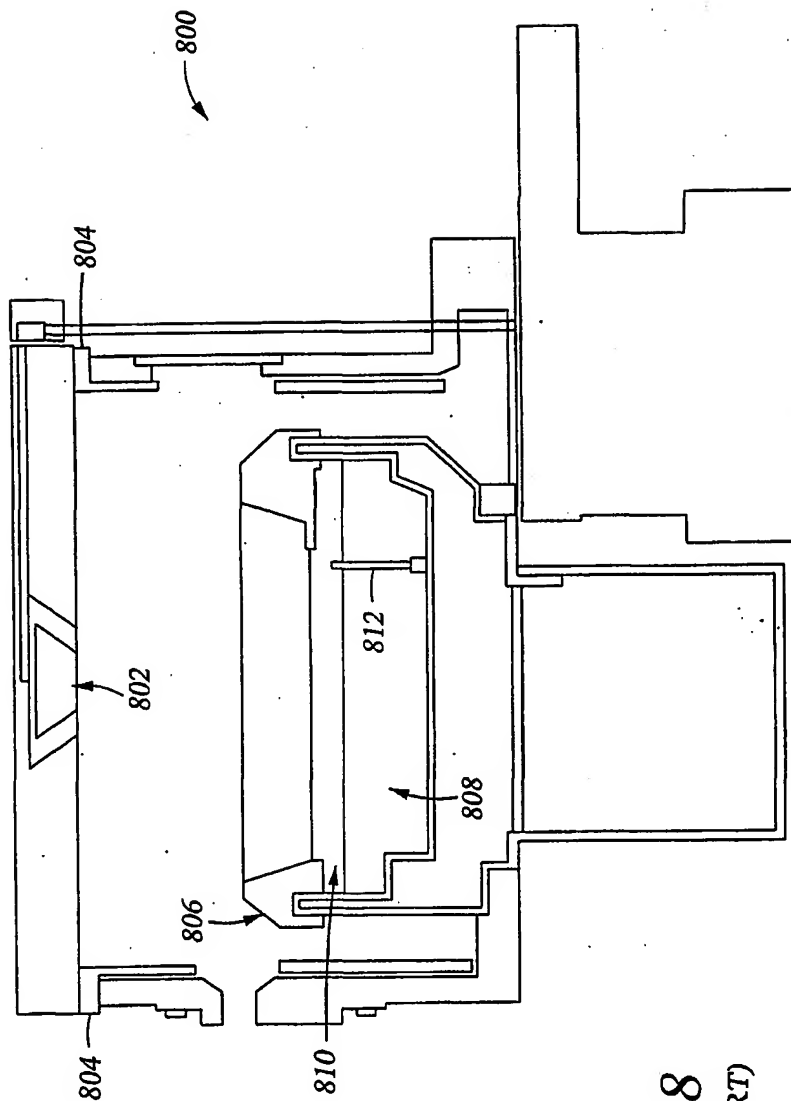


Fig. 8
(PRIOR ART)

INTERNATIONAL SEARCH REPORT

International Application No.
PCT/US 02/07925

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/027

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

PAJ, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 859 400 A (TEXAS INSTRUMENTS) 19 August 1998 (1998-08-19) cited in the application abstract	1-36
A	EP 0 848 416 A (TEXAS INSTRUMENTS) 17 June 1998 (1998-06-17) abstract	1-36
A	WO 99 30360 A (APPLIED MATERIALS) 17 June 1999 (1999-06-17) abstract	1-36

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the International search

28 August 2002

Date of mailing of the international search report

04/09/2002

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International Application No
PCT/US 02/07925

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